

CLAIM LISTING:

1. (Previously Presented) A circuit for determining addresses for reference pixels, said circuit comprising:

an input for receiving parameters, the parameters comprising a picture type indicator for indicating a type of a picture; and

logic for determining whether the parameters received by the input are valid, wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input.

2. (Previously Presented) The circuit of claim 1, further comprising:

an arithmetic logic unit for calculating one or more addresses depending on whether the logic determines that the addresses are valid.

3. (Cancelled)

4. (Previously Presented) The circuit of claim 1, further comprising:

a control register for providing the type of pictures and indicating the number of motion vectors received to the logic.

5. (Previously Presented) The circuit of claim 4, further comprising:

one or more motion vector registers for storing motion vectors received by the input; and

wherein the control register comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector.

6. (Original) The circuit of claim 5, wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state.

7. (Original) The circuit of claim 5, wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B-picture and less than two of the one or more bits are in the particular state.

8. (Previously Presented) A method for determining addresses for reference pixels, said method comprising:

receiving parameters at a video decoder, the parameters comprising a picture type indicator for indicating a type of a picture; and

determining the validity of the parameters, wherein determining the validity of the parameters is based on the picture type indicator, whether the picture is interlaced or progressive, whether the picture is frame predicted or field predicted, and the number of motion vectors received; and

calculating one or more addresses after determining the validity of the parameters, if the parameters are valid.

9. (Original) The method of claim 8, further comprising:

fetching pixels from the one or more addresses after determining the validity of the parameters, if the parameters are valid.

10. (Cancelled)

11. (Previously Presented) The method of claim 8, wherein determining the validity of the parameters further comprises determining that the parameters are invalid if the type of picture is an I-picture and any motion vectors are received.

12. (Currently Amended) The method of claim 8 [10], wherein determining the validity of the parameters further comprises determining that the parameters are invalid if the

control register indicates that the type of picture is a B-picture and less than two of the one or more bits are in the particular state.

13. (Previously Presented) A video decoder for decoding macroblocks, said video decoder comprising:

a processor for decoding a set of parameters, said set of parameters comprising:

a picture type parameter indicating a type of picture; and

motion vectors indicating reference pixels associated with the macroblock;

a motion vector address computer for determining the validity of the set of parameters, and calculating addresses associated with motion vectors if the set of parameters are valid, wherein the motion vector address computer determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is frame predicted, field predicted, dual prime, or 16x8 motion compensation, and the number of motion vectors received by the input; and

a video request manager for fetching reference pixels at the addresses calculated by the motion vector address computer, if the motion vector address computer determines that the set of parameters are valid.

14. (Original) The video decoder of claim 13, wherein the motion vector address computer further comprises:

an input for receiving parameters, the parameters comprising a picture type indicator for indicating a type of a picture; and

logic for determining whether the parameters received by the input are valid.

15. (Original) The video decoder of claim 14, wherein the motion vector address computer further comprises:

an arithmetic logic unit for calculating one or more addresses after the logic determines that the addresses are valid.

16. (Cancelled)

17. (Previously Presented) The video decoder of claim 13, wherein the motion vector address computer further comprises:

a control register for providing the type of pictures and indicating the number of motion vectors received to the logic.

18. (Previously Presented) The video decoder of claim 17, wherein the motion vector address computer further comprises:

one or more motion vector registers for storing motion vectors received by the input; and

wherein the control register comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector.

19. (Original) The video decoder of claim 18, wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state.

20. (Original) The video decoder of claim 18, wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B-picture and less than two of the one or more bits are in the particular state.

21. (New) The video decoder of claim 13, further comprising a control register, said control register comprising one or more bits, each of which are associated with a corresponding one of one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector.